

28

Semiconductor Electronics

TOPIC 1

Semiconductor and p - n Junction Diode

01 The electron concentration in an n -type semiconductor is the same as hole concentration in a p -type semiconductor. An external field (electric) is applied across each of them. Compare the currents in them. [NEET 2021]

- (a) Current in n -type = Current in p -type
- (b) Current in p -type > Current in n -type
- (c) Current in n -type > Current in p -type
- (d) No current will flow in p -type. current will only flow in n -type

Ans. (c)

Given, the electron concentration in n -type semiconductor is equal to the hole's concentration in p -type semiconductor.

When electric field is applied across the semiconductor, the electrons and holes will move opposite to each other. The mobility of n -type semiconductor is greater than mobility of p -type semiconductor.

So, the current in the n -type semiconductor is greater than current in the p -type semiconductor.

02 Consider the following statements (A) and (B) and identify the correct answer.

(A) A Zener diode is connected in reverse bias, when used as a voltage regulator. [NEET 2021]

(B) The potential barrier of p - n junction lies between 0.1 V to 0.3 V.

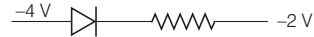
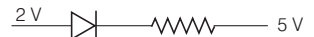


- (a) (A) and (B) both are correct.
- (b) (A) and (B) both are incorrect.

- (c) (A) is correct and (B) is incorrect.
- (d) (A) is incorrect but (B) is correct.

Ans. (c)

Zener diode is a type of special p - n junction diode that operates in reverse bias. Thus, it is used as a voltage regulator. So, the statement (A) is correct. The potential barrier of p - n junction for silicon is 0.6-0.7 V and for germanium is 0.2-0.35 V. So, the statement (B) is incorrect.

03 Out of the following which one is a forward biased diode? [NEET (Oct.) 2020]

- (a) 
- (b) 
- (c) 
- (d) 

Ans. (d)

A p - n junction diode is in forward biased when p -side is connected with more positive potential than n -side.

Since, $0V > -3V$.

Hence in option (d), diode circuit is in forward biased.

04 An intrinsic semiconductor is converted into n -type extrinsic semiconductor by doping it with [NEET (Oct.) 2020]

- (a) phosphorous
- (b) aluminium
- (c) silver
- (d) germanium

Ans. (a)

When a pentavalent (phosphorous) impurities is doped with intrinsic semiconductor (Ge, Si), then n -type semiconductor is formed.

05 The increase in the width of the depletion region in a p - n junction diode is due to [NEET (Sep.) 2020]

- (a) reverse bias only
- (b) both forward bias and reverse bias
- (c) increase in forward current
- (d) forward bias only

Ans. (a)

Under reverse bias condition, the holes of p -side are attracted towards the negative terminal of the battery and electrons of the n -side are attracted towards the positive terminal of the battery. This increases the width of the depletion layer.

However, in the case of forward biasing, the width of the depletion layer decreases. Hence, correct option is (a).

06 The solids which have the negative temperature coefficient of resistance are [NEET (Sep.) 2020]

- (a) insulator only
- (b) semiconductors only
- (c) insulators and semiconductors
- (d) metals

Ans. (c)

Insulators and semiconductors are those solids, which have negative temperature coefficient of resistance. As, when temperature increases number of free electrons increases in both insulator and semiconductor.

Hence, correct option is (c).

07 An LED is constructed from a p - n junction diode using GaAsP. The energy gap is 1.9 eV. The wavelength of the light emitted will be equal to [NEET (Odisha) 2019]

- (a) 10.4×10^{-26} m
- (b) 654 nm
- (c) 654 Å
- (d) 654×10^{-11} m

Ans. (b)

The energy of light of wavelength λ is given by

$$E = h\nu = \frac{hc}{\lambda} \Rightarrow \lambda = \frac{hc}{E} \quad \dots(i)$$

Here, h = Planck's constant

$$= 6.63 \times 10^{-34} \text{ J-s}$$

c = speed of light = 3×10^8 m/s

E = energy gap = $1.9 \text{ eV} = 1.9 \times 1.6 \times 10^{-19} \text{ J}$

Substituting the given values in Eq. (i), we get

$$\Rightarrow \lambda = \frac{6.63 \times 10^{-34} \times 3 \times 10^8}{1.9 \times 1.6 \times 10^{-19}} \\ = 6.54 \times 10^{-7} \text{ m} \approx 654 \text{ nm}$$

Thus, the wavelength of light emitted from LED will be 654 nm.

08 For a p -type semiconductor, which of the following statements is true? [NEET (National) 2019]

- (a) Holes are the majority carriers and trivalent atoms are the dopants.
- (b) Holes are the majority carriers and pentavalent atoms are the dopants.
- (c) Electrons are the majority carriers and pentavalent atoms are the dopants.
- (d) Electrons are the majority carriers and trivalent atoms are the dopants.

Ans. (a)

p -type semiconductors are obtained when a trivalent impurity (e.g. boron, aluminium, gallium or indium) is added to an intrinsic semiconductor. (e.g. germanium or silicon).

In other words, the dopants in p -type semiconductor is trivalent atom.

Thus, this addition creates deficiencies of valence electron which are most commonly known as holes. These are the majority charge carriers in this type of semiconductor. However, in n -type semiconductors, the dopants are pentavalent impurities. Also, the majority charge carriers are electrons.

09 In a p - n junction diode, change in temperature due to heating [NEET 2018]

- (a) does not affect resistance of p - n junction
- (b) affects only forward resistance
- (c) affects only reverse resistance
- (d) affects the overall V - I characteristics of p - n junction

Ans. (d)

Due to increase in temperature because of heating, thermal collision between the

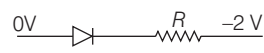


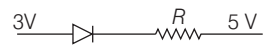
electron and holes increases. Thus, net electron-hole pairs increase.

This leads to increase in the current in diode and overall resistance of the diode changes.

This in turn changes both the forward biasing and the reverse biasing.

Thus, the overall I - V characteristics of p - n junction diode gets affected.

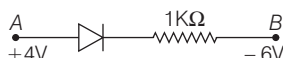
10 Which one of the following represents forward bias diode? [NEET 2017]

- (a) 
- (b) 
- (c) 
- (d) 

Ans. (a)

In the forward biasing of P - N junction, p side of junction diode is connected to higher potential and n side of junction diode is connected to lower potential. Hence, the option (a) is correct answer.

11 Consider the junction diode as ideal. The value of current flowing through AB is [NEET 2016]



- (a) 10^{-2} A
- (b) 10^{-1} A
- (c) 10^{-3} A
- (d) 0 A

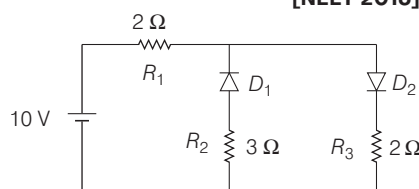
Ans. (a)

Let us assume that current through the diode is I .

From the given condition

$$\therefore I = \frac{V_A - V_B}{R} = \frac{4 - (-6)}{1\text{K}\Omega} \\ = \frac{10}{1 \times 10^3} = 10^{-2} \text{ A}$$

12 The given circuit has two ideal diodes connected as shown in the figure below. The current flowing through the resistance R_1 will be [NEET 2016]



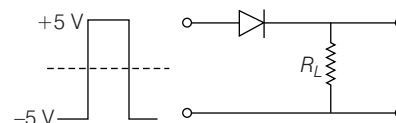
- (a) 2.5 A
- (b) 10.0 A
- (c) 1.43 A
- (d) 3.13 A

Ans. (a)

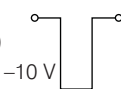
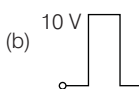


We know that a diode only conducts in forward biased condition. In the given circuit, the diode D_1 will be in reverse bias, so it will block the current and diode D_2 will be in forward bias, so it will pass the current

$$i = \frac{V}{R_1 + R_3} = \frac{10}{2 + 2} = 2.5 \text{ A}$$

13 If in a p - n junction, a square input signal of 10 V is applied as shown, [CBSE AIPMT 2015]



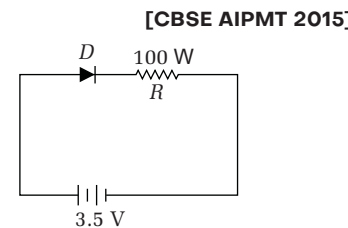
then the output across R_L will be

- (a) 
- (b) 
- (c) 
- (d) 

Ans. (d)

As it is forward biased so it takes positive value. Hence, option (d) is correct.

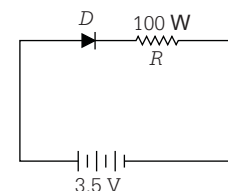
14 In the given figure, a diode D is connected to an external resistance $R = 100 \Omega$ and an e.m.f of 3.5 V. If the barrier potential developed across the diode is 0.5 V, the current in the circuit will be [CBSE AIPMT 2015]



- (a) 30 mA
- (b) 40 mA
- (c) 20 mA
- (d) 35 mA

Ans. (a)

Given, external resistance $R = 100 \Omega$ and an emf is 3.5 V.



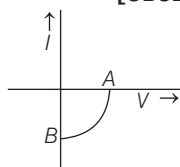
Potential barrier across the diode is 0.5 V,

Potential difference on
 $R = 3.5 \text{ V} - 0.5 \text{ V} = 3.0 \text{ V}$

Current in circuit,

$$I = \frac{V}{R} = \frac{3}{100} \\ = 0.03 \text{ A} = 30 \text{ mA}$$

- 15** The given graph represents V - I characteristic for a semiconductor device. Which of the following statement is correct?
[CBSE AIPMT 2014]



- (a) It is V - I characteristic for solar cell where point A represents open circuit voltage and point B short circuit current
- (b) It is for a solar cell and points A and B represent open circuit voltage and current, respectively
- (c) It is for a photodiode and points A and B represent open circuit voltage and current, respectively
- (d) It is for a LED and points A and B represent open circuit voltage and short circuit current respectively

Ans. (a)

V - I characteristics of a solar cell is shown. Where, A represents open circuit voltage (i.e. $I = 0, V = \text{emf}$) and B shows short circuit voltage (i.e. $I = I, V = 0$).

- 16** The barrier potential of a p - n junction depends on
[CBSE AIPMT 2014]

- (i) type of semiconductor material
- (ii) amount of doping
- (iii) temperature

Which one of the following is correct?

- (a) (i) and (ii) only
- (b) (ii) only
- (c) (ii) and (iii) only
- (d) (i), (ii) and (iii)

Ans. (d)

Barrier potential depends on all the three options given. Barrier potential depends on the material used to make p - n junction diode (whether it is Si or Ge). It also depends on amount of doping due

to which the number of majority carriers will change. It also depends on temperature due to which the number of minority carriers will change.

- 17** In a n -type semiconductor, which of the following statement is true?
[NEET 2013]

- (a) Electrons are majority carriers and trivalent atoms are dopants
- (b) Electrons are minority carriers and pentavalent atoms are dopants
- (c) Holes are minority carriers and pentavalent atoms are dopants
- (d) Holes are majority carriers and trivalent atoms are dopants

Ans. (c)

The n -type semi-conductor can be produced by doping an impurity atom of valency 5 i.e. pentavalent atoms (phosphorus). Holes are minority carriers in them.

- 18** C and Si both have same lattice structure, having 4 bonding electrons in each. However, C is insulator whereas Si is intrinsic semiconductor. This is because
[CBSE AIPMT 2012]

- (a) in case of C, the valence bond is not completely filled at absolute zero temperature
- (b) in case of C, the conduction band is partly filled even at absolute zero temperature
- (c) the four bonding electrons in the case of C lie in the second orbit, whereas in the case of Si they lie in the third
- (d) the four bonding electrons in the case of C lie in the third orbit, whereas for Si they lie in the fourth orbit

Ans. (c)

The four bonding electrons in the case of C lie in the second orbit, whereas in case of Si they lie in the third orbit. So loosely bounded valence electrons are present in Si as compared to C.

- 19** If a small amount of antimony is added to germanium crystal
[CBSE AIPMT 2011]

- (a) the antimony becomes an acceptor atom
- (b) there will be more free electrons than holes in the semiconductor
- (c) its resistance is increased
- (d) it becomes a p -type semiconductor

Ans. (b)

When a small amount of antimony is added to germanium crystal, the crystal becomes n -type semiconductor, because antimony is a pentavalent substrate.

- 20** In forward biasing of the p - n junction
[CBSE AIPMT 2011]

- (a) the positive terminal of the battery is connected to n -side and the depletion region becomes thin
- (b) the positive terminal of the battery is connected to n -side and the depletion region becomes thick
- (c) the positive terminal of the battery is connected to p -side and the depletion region become thin
- (d) the positive terminal of the battery is connected to p -side and the depletion region becomes thick

Ans. (c)

In forward biasing of p - n junction, the positive terminal of the battery is connected to p -side and the depletion region becomes thin.

- 21** Which one of the following statement is false?
[CBSE AIPMT 2010]

- (a) ure Si doped with trivalent impurities gives a p -type semiconductor
- (b) Majority carriers in a n -type semiconductor are holes
- (c) Minority carriers in a p -type semiconductor are electrons
- (d) The resistance of intrinsic semiconductor decreases with increase of temperature.

Ans. (b)

p -type semiconductor are obtained by adding a small amount of trivalent impurity to a pure sample of semiconductor (Ge).

Majority charge carriers—holes
Minority charge carriers—electrons
 n -type semiconductor are obtained by adding a small amount of pentavalent impurity to a pure sample of semiconductor (Ge).

Majority charge carriers—electrons
The resistance of intrinsic semiconductors decreases with increase of temperature.

- 22** Sodium has body centred packing. Distance between two nearest atoms is 3.7 \AA . The lattice parameter is
[CBSE AIPMT 2009, 1999]
- (a) 6.8 \AA (b) 4.3 \AA (c) 3.0 \AA (d) 8.6 \AA

Ans. (b)

Neighbour distance of a body centred cubic cell $d = \frac{\sqrt{3}}{2}a$, where a is the lattice parameter.

$$\Rightarrow 3.7 = \frac{\sqrt{3}a}{2}$$

$$\text{or } a = \frac{2 \times 3.7}{\sqrt{3}} = 4.3 \text{ \AA}$$

23 A p - n photodiode is fabricated from a semiconductor with a band gap of 2.5 eV. It can detect a signal of wavelength [CBSE AIPMT 2009]

- (a) 6000 \AA (b) 4000 \AA
(c) 6000 nm (d) 4000 \AA

Ans. (d)

$$\text{Energy, } E = hv = h \frac{c}{\lambda}$$

$$\Rightarrow \lambda = \frac{hc}{E}$$

Substituting the values of h , c and E in the above equation

$$\lambda = \frac{6.6 \times 10^{-34} \times 3 \times 10^8}{2.5 \times 1.6 \times 10^{-19}} = 5000 \text{ \AA}$$

As $4000 \text{ \AA} < 5000 \text{ \AA}$

Signal of wavelength 4000 \AA can be detected by the photodiode.

24 A p - n photodiode is made of a material with a band gap of 2.0 eV. The minimum frequency of the radiation that can be absorbed by the material is nearly

[CBSE AIPMT 2008]

- (a) 10×10^{14} Hz (b) 5×10^{14} Hz
(c) 1×10^{14} Hz (d) 20×10^{14} Hz

Ans. (b)

Let the energy of radiation falling on the p - n photodiode be $E = hv$

The minimum energy required = 2 eV

$$\therefore 2 \text{ eV} = hv$$

$$\therefore v = \frac{2 \text{ eV}}{h}$$

$$= \frac{2 \times 1.6 \times 10^{-19}}{6.6 \times 10^{-34}}$$

$$= 5 \times 10^{14} \text{ Hz}$$

25 If the lattice parameter for a crystalline structure is 3.6 \AA, then the atomic radius in fcc crystals is [CBSE AIPMT 2008]

- (a) 1.81 \AA (b) 2.10 \AA
(c) 2.92 \AA (d) 1.27 \AA

Ans. (d)

$$\text{For 'fcc' structure, } r = \frac{a}{2\sqrt{2}}$$

where r = radius of the atom in the packing

a = edge length of the cube

Here, $a = 3.6 \text{ \AA}$

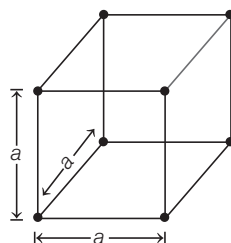
$$\therefore r = \frac{3.6}{2 \times 1.4} = 1.27 \text{ \AA}$$

26 For a cubic crystal structure which one of the following relations indicating the cell characteristic is correct? [CBSE AIPMT 2007]

- (a) $a \neq b \neq c$ and $\alpha \neq \beta$ and $\gamma \neq 90^\circ$
(b) $a \neq b \neq c$ and $\alpha \neq \beta = \gamma = 90^\circ$
(c) $a = b = c$ and $\alpha \neq \beta \neq \gamma = 90^\circ$
(d) $a = b = c$ and $\alpha = \beta = \gamma = 90^\circ$

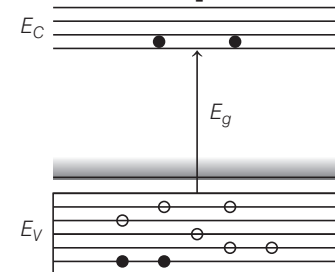
Ans. (d)

In cubic crystals, the crystal axes are perpendicular to one another ($\alpha = \beta = \gamma = 90^\circ$) and the repetitive interval is the same along the three axes ($a = b = c$).



27 In the energy band diagram of a material shown below, the open circles and filled circles denote holes and electrons respectively. The material is a/an

[CBSE AIPMT 2007]



- (a) p -type semiconductor
(b) insulator
(c) metal
(d) n -type semiconductor

Ans. (a)

Since in the given diagram, we see that there are more number of holes so it is ' p ' type semiconductor.

28 A forward biased diode is

[CBSE AIPMT 2006]

Ans.

- (a) (b) (c) (d)

Ans. (d)

The p - n junction diode can be shown as



If p -side of p - n junction diode is given more positive potential or positive terminal of the battery and n -side is connected to less potential or one terminal of battery, then it is forward biased.

In option (d), p -side is at 0 V and n -side at -2 V, so p is at higher potential. Hence, it is forward biased.

p - n junction diode is mainly used as a rectifier.

29 Copper has face-centered cubic (fcc) lattice with interatomic spacing equal to 2.54 \AA. The value of lattice constant for this lattice is [CBSE AIPMT 2005]

- (a) 1.27 \AA
(b) 5.08 \AA
(c) 2.54 \AA
(d) 3.59 \AA

Ans. (d)

Interatomic spacing for a fcc lattice is given by

$$r = \left[\left(\frac{a}{2} \right)^2 + \left(\frac{a}{2} \right)^2 + (0)^2 \right]^{1/2} = \frac{a}{\sqrt{2}}$$

where, a being lattice constant.

$$\therefore a = \sqrt{2}r = \sqrt{2} \times 2.54 = 3.59 \text{ \AA}$$

Interatomic spacing is just the nearest neighbours distance.

30 Choose only false statement from the following [CBSE AIPMT 2005]

- (a) Substances with energy gap of the order of 10 eV are insulators
(b) The conductivity of a semiconductor increases with increases in temperature
(c) In conductors the valence and conduction bands may overlap

- (d) The resistivity of a semiconductor increases with increase in temperature

Ans. (d)

- (a) In insulators, energy gap is of the order of 5 to 10 eV and it is practically impossible to impart this much amount of energy to the electrons in valence band so as to jump to conduction band. So, choice (a) is correct.
- (b) In semiconductors, with the rise in temperature more electrons from valence band jump to conduction band and this results in increase in conductivity. So, choice (b) is correct.
- (c) In conductors, the conduction band is either partially filled or the conduction band overlaps on the valence band. So, choice (c) is correct.
- (d) In semiconductor, resistivity decreases with increase in temperature. So, choice (d) is wrong.

31 Zener diode is used for
[CBSE AIPMT 2005]

- (a) producing oscillations in an oscillator
(b) amplification
(c) stabilisation
(d) rectification

Ans. (c)

Zener diode is a silicon crystal diode having an unusual reverse current characteristic which is particularly suitable for voltage regulating purposes or voltage stabilisation purposes.

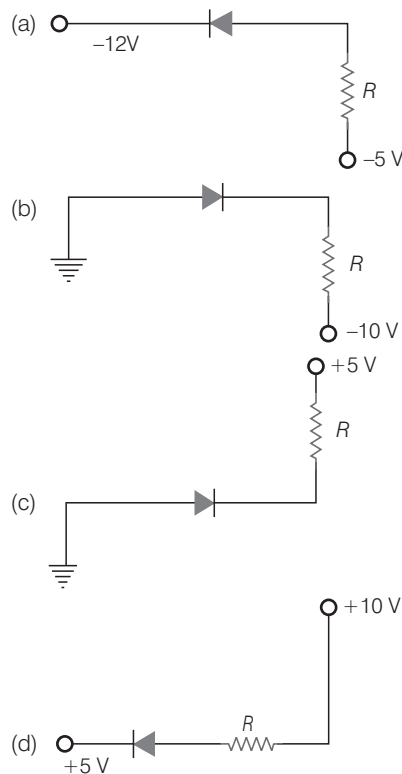
32 Application of a forward bias to a p - n junction [CBSE AIPMT 2005]

- (a) increases the number of donors on the n -side
(b) increases the electric field in the depletion zone
(c) increases the potential difference across the depletion zone
(d) widens the depletion zone

Ans. (a)

On applying forward bias to a p - n junction diode, it increases number of donor on the n -side and decreases potential barrier. It also decreases electric field of depletion layer.

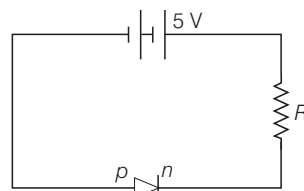
33 Of the diodes shown in the following diagrams, which one is reverse biased? [CBSE AIPMT 2004]



Ans. (c)

When a battery is connected to junction diode with p -side connected to negative terminal or lower potential and n -side to the positive terminal or higher potential, the junction diode is reverse biased.

The circuit shown in figure can be redrawn as



In the option (c), the p -end of the diode is connected to negative terminal of the battery, so the diode has been reverse biased.

34 In a p - n junction photo cell, the value of the photo-electromotive force produced by monochromatic light is proportional to [CBSE AIPMT 2004]

- (a) the barrier voltage at the p - n junction
(b) the intensity of the light falling on the cell
(c) the frequency of the light falling on the cell
(d) the voltage applied at the p - n junction

Ans. (b)

In a photoconductive cell, when monochromatic light is incident on the transparent metallic film, a force produced called the photo electromotive force, stimulates the emission of an electric current where photovoltaic action creates a potential difference between two points.

The magnitude of this current depends upon the intensity of incident light. Hence, photo electromotive force produced by monochromatic light is proportional to the intensity of light falling on the cell.

35 The peak voltage in the output of a half-wave diode rectifier fed with a sinusoidal signal without filter is 10 V. The DC component of the output voltage is [CBSE AIPMT 2004]

- (a) $\frac{10}{\sqrt{2}}$ V
(b) $\frac{10}{\pi}$ V
(c) 10 V
(d) $\frac{20}{\pi}$ V

Ans. (b)

The output DC component of half wave rectifier is given by

$$V_{\text{output}} = \frac{\text{peak voltage}}{\pi} = \frac{10}{\pi}$$

36 In semiconductors at a room temperature [CBSE AIPMT 2004]

- (a) the valence band is partially empty and the conduction band is partially filled
(b) the valence band is completely filled and the conduction band is partially filled
(c) the valence band is completely filled and the conduction band is completely empty
(d) the valence band is completely empty

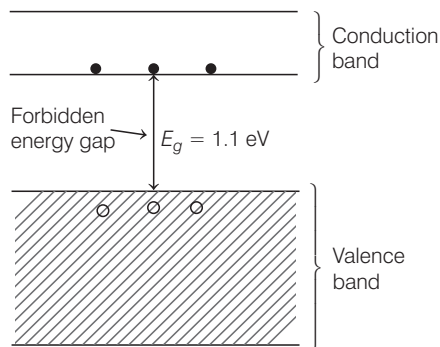
Ans. (a)

The energy band scheme of semiconductors is shown here.

In semiconductors, valence band and conduction band are separated by an energy gap called the forbidden energy gap. It is very small. At room temperature some electrons in valence band acquire thermal energy.

This energy is more than forbidden energy gap E_g , thus they jump into the conduction band and leave their vacancy in the valence band which act as holes.

Hence, at room temperature valence band is partially empty and conduction band is partially filled.



- 37** If a full wave rectifier circuit is operating from 50 Hz mains, the fundamental frequency in the ripple will be [CBSE AIPMT 2003]
- (a) 70.7 Hz (b) 100 Hz
(c) 25 Hz (d) 59 Hz

Ans. (b)

For full wave rectifier,
Ripple frequency = $2 \times$ input frequency
= 2×50
= 100 Hz

- 38** Barrier potential of a p - n junction diode does not depend on [CBSE AIPMT 2003]

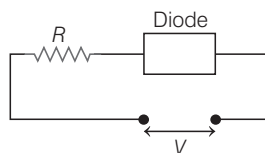
- (a) forward bias
(b) doping density
(c) diode design
(d) temperature

Ans. (c)

Barrier potential does not depend on diode design while it depends on temperature, doping density and forward biasing.

- 39** For a given circuit of ideal p - n junction diode, which of the following is correct?

[CBSE AIPMT 2002]



- (a) In forward biasing the voltage across R is V
(b) In reverse biasing the voltage across R is V
(c) In forward biasing the voltage across R is $2V$
(d) In reverse biasing the voltage across R is $2V$

Ans. (a)

In forward biasing, the diode conducts. For ideal junction diode, the forward resistance is zero. Therefore, entire applied voltage occurs across resistance R

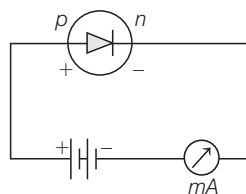
While in reverse biasing, the diode does not conduct, so it has infinite resistance. Thus, voltage across R is zero in reverse biasing.

- 40** For conduction in a p - n junction, the biasing is [CBSE AIPMT 2002]

- (a) high potential on n -side and low potential on p -side
(b) high potential on p -side and low potential on n -side
(c) same potential on both p and n -sides
(d) undetermined

Ans. (b)

For conduction in a p - n junction, it should be forward biased because it offers minimum resistance to the flow of current. For this p -side must be connected to positive terminal (higher potential) and n -side must be connected to negative terminal (lower potential). Figure below shows the p - n junction in a conducting state (forward biased condition)



- 41** The number of atoms per unit cell in bcc lattice is [CBSE AIPMT 2002]

- (a) 1 (b) 2
(c) 4 (d) 9

Ans. (b)

Number of atoms per unit cell is given by

$$N = N_b + \frac{N_f}{2} + \frac{N_c}{8}$$

where N_b = number of atoms centred in the body

N_f = number of atoms centred in the face

N_c = number of atoms centred at the corners

For bcc structure,

$$N_b = 1, N_f = 0$$

and $N_c = 8$

$$\therefore N = 1 + \frac{0}{2} + \frac{8}{8} = 2$$

- 42** In bcc structure of lattice constant a , the minimum distance between atoms is [CBSE AIPMT 2001]

- (a) $\frac{\sqrt{3}}{2}a$ (b) $\sqrt{2}a$ (c) $\frac{a}{\sqrt{2}}$ (d) $\frac{a}{2}$

Ans. (a)

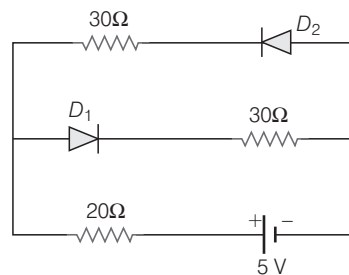
In a bcc structure, the position vectors of the nearest neighbours of the origin are

$$\left(\pm \frac{a}{2} \hat{i}, \pm \frac{a}{2} \hat{j}, \pm \frac{a}{2} \hat{k} \right)$$

The distance between any two nearest neighbours is given but the resultant of above position vector is

$$\sqrt{\left(\frac{a}{2}\right)^2 + \left(\frac{a}{2}\right)^2 + \left(\frac{a}{2}\right)^2} = \sqrt{\frac{3a^2}{4}} = \frac{\sqrt{3}}{2}a$$

- 43** If internal resistance of cell is negligible, then current flowing through the circuit is [CBSE AIPMT 2001]



- (a) $\frac{3}{50}$ A (b) $\frac{5}{50}$ A
(c) $\frac{4}{50}$ A (d) $\frac{2}{50}$ A

Ans. (b)

In the circuit, diode D_1 is forward biased and diode D_2 is reverse biased.

Therefore, no current flows in the arm containing D_2 and all of the current flows through arm containing D_1 .

Thus, current flowing through the circuit is given by

$$I = \frac{V}{R_{eq}} = \frac{5}{20+30} = \frac{5}{50} \text{ A}$$

$$[\because R_{eq} = 20 \Omega + 30 \Omega]$$

- 44** Si and Cu are cooled to a temperature of 300 K, then resistivity [CBSE AIPMT 2001]

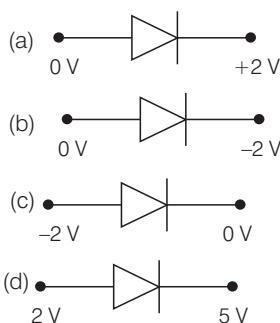
- (a) for Si increases and for Cu decreases
(b) for Cu increases and for Si decreases
(c) decreases for both Si and Cu
(d) increases for both Si and Cu

Ans. (a)

Resistivity of a metal is directly proportional to temperature because its temperature coefficient is positive and resistivity of semiconductor is inversely proportional to temperature. due to its negative temperature coefficient. This implies that with decrease in temperature, resistivity of metal decreases while that of semiconductor increases.

Here, Si is a semiconductor and Cu is a metal. So, resistivity of Si increases but that of Cu decreases.

45 In which of the following figures, junction diode is forward biased ?
[CBSE AIPMT 2000]



Ans. (b)

For forward biasing of p - n junction, p -side should be at higher potential than n -side. Now we apply this rule to the four options.

- (a) Here, p -side is at lower potential (0 V) and n -side at higher potential (2 V). So, this diode is not forward biased.
 - (b) Here, p -side is at higher potential (0 V) and n -side at lower potential (-2 V). So, this diode is forward biased.
 - (c) Here, p -side is at lower potential (-2 V) and n -side at higher potential (0 V). So, this diode is not forward biased.
 - (d) Here p -side is at lower potential (2 V) and n -side at higher potential (5 V). So, this is not forward biased.
- Hence, choice (b) is correct.

46 In p -type semiconductor, the majority charge carriers are
[CBSE AIPMT 1999]

- (a) holes
- (b) electrons
- (c) protons
- (d) neutrons

Ans. (a)

Semiconductors doped with acceptor atoms are called p -type

semiconductors. The p stands for positive to imply that the holes are introduced into the valence band, which behave like positive charge carriers, greatly in number than the electrons in the conduction band.

In p -type semiconductors, holes are the majority carriers and electrons are the minority carriers.

47 In forward bias the width of depletion layer in a p - n junction diode
[CBSE AIPMT 1999]

- (a) increases
- (b) decreases
- (c) remains constant
- (d) first increases then decreases

Ans. (b)

Since in forward biasing, negative of the battery is connected to n -type side, and the positive terminal of battery is connected to p -type side hence an electric field is created in direction opposite to the \mathbf{E} in the potential barrier region. Thus, depletion layer of p - n junction diode decreases.

48 Depletion layer consists of
[CBSE AIPMT 1999]

- (a) electrons
- (b) protons
- (c) mobile charge carriers
- (d) immobile ions

Ans. (d)

When a piece of p -type material is in contact with n -type material, then to bring Fermi level in a line, electrons in conduction band on n -type side travel across the junction and leave the positively ionised impurity atoms unneutralized. Consequently, there is a positively charged region adjacent to the junction in n -type material.

On p -type side, the electrons which have traversed the boundary recombine with positive holes in the valence band. Near to the junction on p -type side, there is a layer of unneutralised negatively ionised trivalent impurity which forms a negatively charged region. This region around the junction is called charge depletion region or space charge region.

49 In a junction diode, the holes are due to
[CBSE AIPMT 1999]

- (a) protons
- (b) extra electrons
- (c) neutrons
- (d) missing electrons

Ans. (d)

In a junction diode, when electron jumps to conduction band from valence band due to thermal agitation or any other

circumstances, then a vacancy is created in valence band which has positive charge equal to charge of electron in magnitude. This is called a hole.

Thus, holes in junction diode are due to missing electrons.

50 Which of the following when added as an impurity into silicon produces n -type semiconductor ?
[CBSE AIPMT 1999]

- (a) P
- (b) Al
- (c) B
- (d) Mg

Ans. (a)

When pentavalent impurity is added to silicon then n -type semiconductor is formed. Out of given options, only phosphorus (P) is pentavalent, so it should be doped to silicon to make it n -type semiconductor.

51 A semiconducting device is connected in a series in circuit with a battery and a resistance. A current is allowed to pass through the circuit. If the polarity of the battery is reversed, the current drops to almost zero. The device may be
[CBSE AIPMT 1998]

- (a) a p - n junction
- (b) an intrinsic semiconductor
- (c) a p -type semiconductor
- (d) an n -type semiconductor

Ans. (a)

We know that in forward biasing of p - n junction the current is of the order of milliampere while in reverse biasing the current is of the order of microampere (negligible). Thus, device is a p - n junction.

52 The cause of the potential barrier in a p - n diode is
[CBSE AIPMT 1998]

- (a) depletion of positive charges near the junction
- (b) concentration of positive charges near the junction
- (c) depletion of negative charges near the junction
- (d) concentration of positive and negative charges near the junction

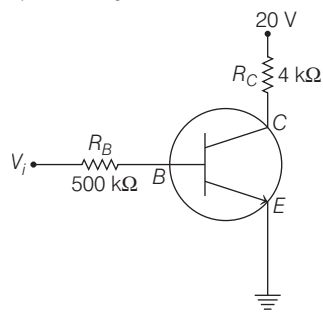
Ans. (d)

In a p - n junction diode, majority carriers are holes on p -side and electrons on n -side. Holes, thus diffuse to n -side and electrons to p -side. This diffusion causes a layer of positive charge in the

n -region and layer of negative charge in the p -region near the junction.

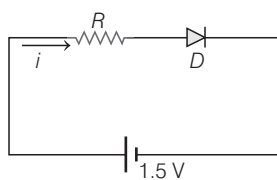
This double layer of opposite charge creates an electric field which exerts a force on the electrons and holes, against their diffusion. This electric field becomes strong enough as diffusion proceeds to stop it. In the equilibrium position, there is a barrier, for charge motion with the n -side at a higher potential than the p -side.

The junction region has a very low density of either p or n -type carriers, because of inter diffusion. It is called depletion region.



- 53** The diode used in the circuit shown in the figure has a constant voltage drop of 0.5 V at all currents and a maximum power rating of 100 milliwatt. What should be the value of the resistor R , connected in series with the diode, for obtaining maximum current i ?

[CBSE AIPMT 1997]



- (a) 200 Ω (b) 6.67 Ω
(c) 5 Ω (d) 15 Ω

Ans. (c)

$$\text{Current in circuit } i = \frac{P}{V_d} = \frac{100 \times 10^{-3}}{0.5}$$

$$[V_d = \text{voltage drop across diode}] = 200 \times 10^{-3} \text{ A}$$

$$\text{Voltage across resistance } R, V' = 1.5 - 0.5 = 1.0 \text{ V}$$

$$\text{Thus, resistance } R = \frac{V'}{i} = \frac{1}{200 \times 10^{-3}} = 5 \Omega$$

- 54** To obtain a p -type germanium semiconductor, it must be doped with [CBSE AIPMT 1997]

- (a) phosphorus (b) indium
(c) antimony (d) arsenic

Ans. (b)

If a trivalent impurity is mixed in a pure (intrinsic) semiconductor, then it becomes a p -type semiconductor. As given indium is trivalent impurity so it must be doped to Ge or Si to make it p -type semiconductor.

- 55** When arsenic is added as an impurity to silicon, the resulting material is [CBSE AIPMT 1996]

- (a) n -type semiconductor
(b) p -type semiconductor
(c) n -type conductor
(d) insulator

Ans. (a)

When a small amount of pentavalent impurity is added to a pure semiconductor, it is known as n -type semiconductor. Arsenic (33) is pentavalent impurity. The addition of pentavalent impurity provides a large number of free electrons in the semiconductor crystal.

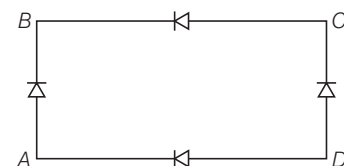
- 56** Which of the following, when added as an impurity, into the silicon, produces n -type semiconductor? [CBSE AIPMT 1995]

- (a) Phosphorus (b) Aluminium
(c) Magnesium (d) Both (b) and (c)

Ans. (a)

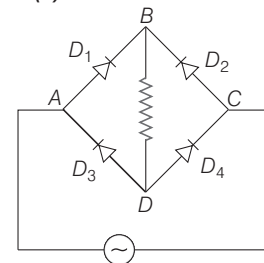
When a small amount of pentavalent impurity is added to a pure semiconductor, it is known as n -type semiconductor. Phosphorus (P) is a pentavalent and silicon is a tetravalent. Therefore, when phosphorus is doped with Si, it forms a n -type semiconductor.

- 57** In figure the input is across the terminals A and C and the output is across B and D . Then the output is [CBSE AIPMT 1994]

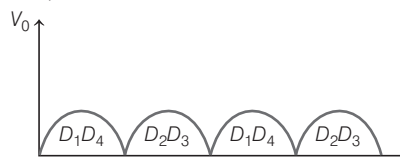


- (a) zero
(b) same as the input
(c) half wave rectified
(d) full wave rectified

Ans. (d)



AC input is applied across A and C and output is taken across BD .



When positive cycle is fed to AC , D_1 and D_4 conduct, when negative cycle is fed to AC , D_3 and D_2 conduct in the same direction. Output across BD is thus full wave rectified.

- 58** When a p - n junction diode is reverse biased the flow of current across the junction is mainly due to [CBSE AIPMT 1994]

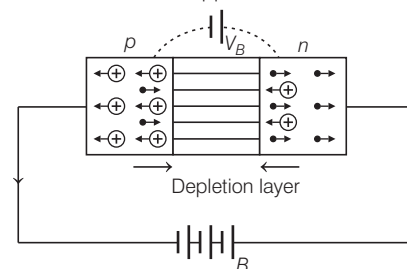
- (a) diffusion of charges
(b) drift charges
(c) Depends on the nature of material
(d) Both drift and diffusion of charges

Ans. (b)

A p - n junction is said to be reverse biased, if the positive terminal of the external battery B is connected to n -side and the negative terminal to p -side of the p - n junction.

In reverse biasing, the reverse bias voltage supports the potential barrier V_B . Now the majority carriers are pulled away from the junction and the depletion region becomes thick.

There is no conduction across the junction due to majority carriers. However, a few minority carriers (holes in n -section and electrons in p -section) of p - n junction diode cross the junction after being accelerated by high reverse bias voltage. They constitute a current that flows in the opposite direction.



So when p - n junction is reverse biased, the flow of current is due to drifting of minority charge carries across the junction.

59 A piece of copper and other of germanium are cooled from the room temperature to 80 K, then
[CBSE AIPMT 1993]

- (a) resistance in each will increase
- (b) resistance in each will decrease
- (c) the resistance of copper will increase while that of germanium will decrease
- (d) the resistance of copper will decrease while that of germanium will increase

Ans. (d)

Semiconductor have negative temperature coefficient of resistance i.e. the resistance of a semiconductor decreases with the increase in temperature as no. of electrons increases in conduction band. Copper has positive temperature coefficient of resistance, i.e. the resistance of copper increases with the increase in temperature due to the collision of electrons. Hence, at 80 K, the resistance of copper will decrease while that of germanium will increase.

60 Diamond is very hard, because
[CBSE AIPMT 1993]

- (a) it is covalent solid
- (b) it has large cohesive energy
- (c) high melting point
- (d) insoluble in all solvents

Ans. (b)

The cohesive energy of solids is defined as the energy required for separating the condensed material into isolated free atoms.

The bond between two carbon atoms in diamond has a cohesive energy of 7.3 eV with respect to separated neutral atoms. Due to such high cohesive energy diamond is very hard.

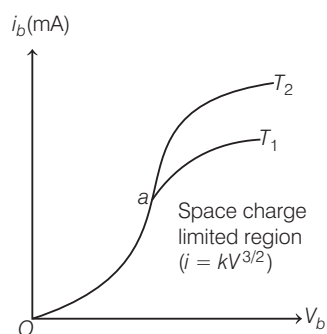
61 For an electronic valve, the plate current i and plate voltage V in the space charge limited region are related as
[CBSE AIPMT 1992]

- (a) i is proportional to $V^{3/2}$
- (b) i is proportional to $V^{2/3}$
- (c) i is proportional to V
- (d) i is proportional to V^2

Ans. (a)

The most important characteristic of a vacuum diode is the plate characteristic which gives the relation between plate voltage and plate current for a given cathode temperature.

It may be noted from the plate characteristics that all the curves are coincident at low plate voltage where the negative space charge is most effective in limiting plate current. This low plate voltage region [region oa in figure] is known as space charge limited region. In this region, the plate current increases as the plate voltage is increased, because more positive plate attracts electrons from the space charge at a greater rate. In the space charge limited region the plate current is given by the relation $i = kV^{3/2}$



i.e. $i \propto V^{3/2}$
where, k is constant.

62 Which one of the following is the weakest kind of the bonding in solids?
[CBSE AIPMT 1992]

- (a) Ionic
- (b) Metallic
- (c) van der Waals'
- (d) Covalent

Ans. (c)

Many solids or crystals are composed of neutral atoms or molecules without any transferring, sharing or free movement of electrons. These solids remains bound by much weaker, short range attractive forces, known as 'van der Waals' forces. These forces arise as a result of fluctuations in the charge distributions of nearby molecules.

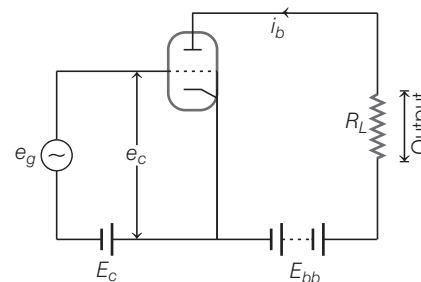
63 For amplification by a triode, the signal to be amplified is given to
[CBSE AIPMT 1992]

- (a) the cathode
- (b) the grid
- (c) the glass-envelope
- (d) the anode

Ans. (b)

Figure shows the basic triode amplifier circuit. The weak signal e_g is applied in the grid circuit and useful output is obtained across the load R_L connected in the plate circuit. The bias battery E_c ensures the grid to be always negative w.r.t. cathode.

The weak signal voltage produces a large change in plate current. As the value of R_L is quite high, therefore a large voltage drop occurs across it. Thus, a weak signal applied in the grid circuit appears in the amplified form in the plate circuit.

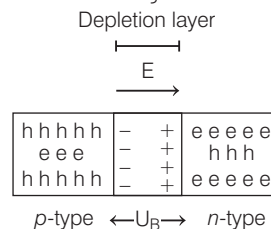


64 The depletion layer in the p - n junction region is caused by
[CBSE AIPMT 1991]

- (a) drift of holes
- (b) diffusion of charge carriers
- (c) migration of impurity ions
- (d) drift of electrons

Ans. (b)

The accumulation of electric charges of opposite polarities in the two regions of the junction gives rise to an electric field between these region due to the diffusion of charge carriers. This electric field opposes further flow of electrons from the n -region to the p -region and that of holes from the p -region to n -region. This electric field sets a potential barrier V_B at the junction which opposes further diffusion of free charge carriers into opposite regions. In the vicinity of the junction, a region is created, which is devoid of free charge carriers and has immobile ions. This region in which no free charge carriers are available is called a depletion region. This is shown in figure.



65 When a triode is used as an amplifier the phase difference between the input signal voltage and the output is

[CBSE AIPMT 1990]

- (a) zero (b) π
 (c) $\frac{\pi}{2}$ (d) $\frac{\pi}{4}$

Ans. (b)

In the triode amplifier, there is a phase difference of 180° between the input (i.e. signal) voltage and output voltage. In other words, the positive half-cycle of the signal appears as amplified negative-half in the output while the negative half-cycle of the signal appears as amplified positive half in the output.

This is known as phase reversal. In other words, as the signal is increasing in the negative half-cycle, the output is increasing in the positive sense.

66 When n -type semiconductor is heated [CBSE AIPMT 1989]

- (a) number of electrons increases while that of holes decreases
 (b) number of holes increases while that of electrons decreases
 (c) number of electrons and holes remain same
 (d) number of electrons and holes increases equally

Ans. (d)

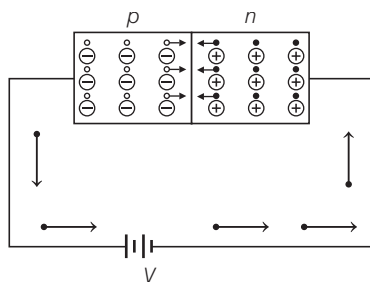
When n -type semiconductor is heated a few hole-electron pairs generate. When a free electron is produced then simultaneously a hole is also produced. Thus no. of electrons and holes both increases equally.

67 p - n junction is said to be forward biased, when [CBSE AIPMT 1988]

- (a) the positive pole of the battery is joined to the p -semiconductor and negative pole to the n -semiconductor
 (b) the positive pole of the battery is joined to the n -semiconductor and negative pole to the p -semiconductor
 (c) the positive pole of the battery is connected to n -semiconductor and p -semiconductor
 (d) a mechanical force is applied in the forward direction

Ans. (a)

When external voltage is applied to the junction in such a direction that it cancels the potential barrier, or decreases potential barrier thus permitting current flow, it is called forward biasing. To apply forward bias, connect positive terminal of the battery to p -type and negative terminal to n -type as shown in figure.



68 At absolute zero, Si acts as

[CBSE AIPMT 1988]

- (a) non-metal (b) metal
 (c) insulator (d) None of these

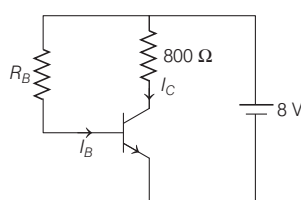
Ans. (c)

Semiconductors have negative temperature coefficient of resistance, i.e. the resistance of a semiconductor decreases with the increase in temperature and *vice-versa*. Silicon is actually an insulator at absolute zero of temperature but it becomes a good conductor at high temperatures. Because on giving temperatures to semiconductor some of the electron jumps from valence band to conduction band.

TOPIC 2 Transistors

69 A n - p - n transistor is connected in common emitter configuration (see figure) in which collector voltage drop across load resistance (800Ω) connected to the collector circuit is 0.8 V. The collector current is

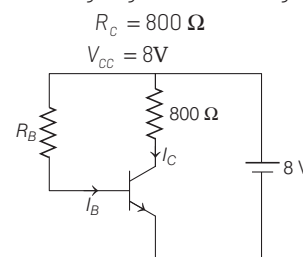
[NEET (Oct.) 2020]



- (a) 2 mA (b) 0.1 mA (c) 1 mA (d) 0.2 mA

Ans. (c)

According to given circuit diagram.



Voltage drop across R_C ,

$$V_C = 0.8V$$

$$\Rightarrow I_C R_C = 0.8$$

$$I_C = \frac{0.8}{R_C} = \frac{0.8}{800} = 10^{-3} A = 1 \text{ mA}$$

70 For transistor action, which of the following statements is correct?

[NEET (Sep.) 2020]

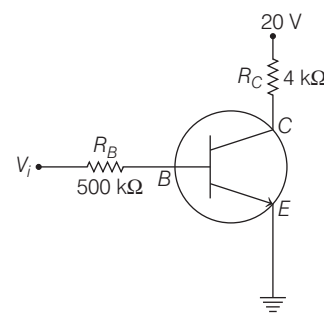
- (a) Base, emitter and collector regions should have same size.
 (b) Both emitter junction as well as the collector junction are forward biased.
 (c) The base region must be very thin and lightly doped.
 (d) Base, emitter and collector regions should have same doping concentrations.

Ans. (c)

In case of transistor action, base region is thin and lightly doped. While, emitter region is heavily doped and collector region is moderately doped. Also, the size of collector is slightly more than the size of emitter.

Hence, option (c) is correct.

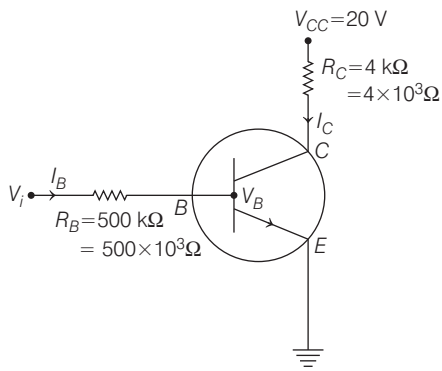
71 In the circuit shown in the figure, the input voltage V_i is 20 V, $V_{BE} = 0$ and $V_{CE} = 0$. The values of I_B , I_C and β are given by [NEET 2018]



- (a) $I_B = 20 \mu\text{A}$, $I_C = 5 \text{ mA}$, $\beta = 250$
 (b) $I_B = 25 \mu\text{A}$, $I_C = 5 \text{ mA}$, $\beta = 200$
 (c) $I_B = 40 \mu\text{A}$, $I_C = 10 \text{ mA}$, $\beta = 250$
 (d) $I_B = 40 \mu\text{A}$, $I_C = 5 \text{ mA}$, $\beta = 125$

Ans. (d)

Given, $V_{BE} = 0 \text{ V}$, $V_{CE} = 0 \text{ V}$ and $V_i = 20 \text{ V}$



Applying Kirchhoff's law to the base-emitter loop, we get

$$V_i = I_B R_B + V_{BE}$$

Substituting the values, we get

$$20 = I_B \times (500 \times 10^3) + 0$$

$$\Rightarrow I_B = \frac{20}{500 \times 10^3} = 0.04 \times 10^{-3}$$

$$= 40 \times 10^{-6} = 40 \mu\text{A} \quad \dots(i)$$

Similarly, $V_{CC} = I_C R_C + V_{CE}$

Substituting the given values, we get

$$20 = I_C \times (4 \times 10^3) + 0$$

$$\Rightarrow I_C = \frac{20}{4 \times 10^3} = 5 \times 10^{-3} = 5 \text{ mA} \quad \dots(ii)$$

Current gain is given as

$$\beta = \frac{I_C}{I_B}$$

Substituting the value of I_B and I_C from Eqs. (i) and (ii), we get

$$\Rightarrow \beta = \frac{5 \times 10^{-3}}{40 \times 10^{-6}} = 0.125 \times 10^3$$

$$= 125$$

72 In a common emitter transistor amplifier, the audio signal voltage across the collector is 3 V. The resistance of collector is 3 kΩ. If current gain is 100 and the base resistance is 2 kΩ, the voltage and power gain of the amplifier is

[NEET 2017]

- (a) 200 and 1000 (b) 15 and 200
 (c) 150 and 15000 (d) 20 and 2000

Ans. (c)

Collector current $i_c = \frac{V}{R} = \frac{3}{3 \times 10^3} = 10^{-3} \text{ A}$

Now base current

$$i_B = \frac{i_C}{\beta} = \frac{10^{-3}}{100} = 10^{-5} \text{ A}$$

As, voltage $V_{in} = i_B R_B$

$$\therefore V_{in} = 10^{-5} \times 2 \times 10^3 = 2 \times 10^{-2} \text{ volts}$$

$$\text{So, voltage gain } A_V = \frac{V_{out}}{V_{in}} = \frac{3}{2 \times 10^{-2}}$$

$$= 150$$

$$\text{Power gain} = A_V \times \beta = 150 \times 100 = 15000$$

73 A *n-p-n* transistor is connected in common emitter configuration in a given amplifier. A load resistance of 800 Ω is connected in the collector circuit and the voltage drop across it is 0.8 V. If the current amplification factor is 0.96 and the input resistance of the circuit is 192 Ω, the voltage gain and the power gain of the amplifier will respectively be [NEET 2016]

- (a) 3.69, 3.84 (b) 4, 4
 (c) 4, 3.69 (d) 4, 3.84

Ans. (d)

Given, resistance across load, $R_L = 800 \Omega$

Voltage drop across load, $V_L = 0.8 \text{ V}$

Input resistance of circuit, $R_i = 192 \Omega$.

Collector current is given by,

$$I_C = \frac{V_L}{R_L} = \frac{0.8}{800} = \frac{8}{8000} = 1 \text{ mA}$$

\therefore Current amplification

$$= \frac{\text{Output current}}{\text{Input current}} = \frac{I_C}{I_B} = 0.96 \Rightarrow I_B = \frac{1 \text{ mA}}{0.96}$$

\therefore Voltage gain,

$$A_V = \frac{V_L}{V_{in}} = \frac{V_L}{I_B R_i} = \frac{0.8 \times 0.96}{10^{-3} \times 192} = 4$$

$\Rightarrow A_V = 4$

and Power gain,

$$A_P = \frac{I_C^2 R_L}{I_B^2 R_i} = \left(\frac{I_C}{I_B}\right)^2 \cdot \frac{R_L}{R_i} = (0.96)^2 \times \frac{800}{192}$$

$$A_P = 3.84$$

74 For CE transistor amplifier, the audio signal voltage across the collector resistance of 2 kΩ is 4 V. If the current amplification factor of the transistor is 100 and the base resistance is 1 kΩ, then the input signal voltage is [NEET 2016]

- (a) 10 mV (b) 20 mV
 (c) 30 mV (d) 15 mV

Ans. (b)

Key Idea Voltage amplification is

$$A_V = \beta \frac{R_{out}}{R_{in}} = \frac{(V_{out})_{AC}}{(V_{in})_{AC}}$$

Given, collector resistance = $R_{out} = 2 \text{ k}\Omega$

Current amplification factor, $\beta = 100$

Base resistance, $R_{in} = 1 \text{ k}\Omega$

Output signal voltage = 4 V

Putting all the values in given equation, we get

$$A_V = \beta \frac{R_{out}}{R_{in}} = 100 \times \frac{2 \text{ k}\Omega}{1 \text{ k}\Omega} \Rightarrow A_V = 200$$

$$\text{Now, } A_V = \frac{(V_{out})_{AC}}{(V_{in})_{AC}} = 200$$

$$\Rightarrow (V_{in})_{AC} = \frac{4}{200} = 20 \text{ mV}$$

75 The input signal given to a CE amplifier having a voltage gain of 150 is $V_i = 2 \cos\left(15t + \frac{\pi}{3}\right)$. The

corresponding output signal will be [CBSE AIPMT 2015]

- (a) $300 \cos\left(15t + \frac{\pi}{3}\right)$
 (b) $75 \cos\left(15t + \frac{2\pi}{3}\right)$
 (c) $2 \cos\left(15t + \frac{5\pi}{3}\right)$ (d) $300 \cos\left(15t + \frac{4\pi}{3}\right)$

Ans. (d)

Input signal of a CE amplifier,

$$V_{in} = 2 \cos\left(15t + \frac{\pi}{3}\right)$$

Voltage gain $A_V = 150$

As CE amplifier gives phase difference of π between input and output signals.

$$\text{So, } A_V = \frac{V_0}{V_{in}} \Rightarrow V_0 = A_V V_{in}$$

$$V_0 = 150 \times 2 \cos\left(15t + \frac{\pi}{3} + \pi\right)$$

$$V = 300 \cos\left(15t + \frac{4\pi}{3}\right)$$

76 In a common emitter (CE) amplifier having a voltage gain G , the transistor used has transconductance 0.03 mho and current gain 25. If the above transistor is replaced with another one with transconductance 0.02 mho and current gain 20, the voltage gain will [NEET 2013]

- (a) $\frac{2}{3}G$ (b) 1.5G
 (c) $\frac{1}{3}G$ (d) $\frac{5}{4}G$

Ans. (a)

As $A_v = \beta \frac{R_L}{R_i}$ or $G = \left(\frac{\beta}{R_i}\right) R_L$

$\Rightarrow G = g_m R_L \Rightarrow G \propto g_m$

$$\left[\because g_m = \frac{\Delta I_c}{\Delta V_B} = \frac{\Delta I_c}{\Delta I_B R_i} \right]$$

$$\left[\because g_m = \frac{\beta}{R_i} \right]$$

$\therefore \frac{G_2}{G_1} = \frac{g_{m2}}{g_{m1}} \Rightarrow G_2 = \frac{0.02}{0.03} \times G$

So, voltage gain, $G_2 = \frac{2}{3}G$

- 77** In a CE transistor amplifier, the audio signal voltage across the collector resistance of 2 k Ω is 2V. If the base resistance is 1k Ω and the current amplification of the transistor is 100, the input signal voltage is **[CBSE AIPMT 2012]**
 (a) 0.1 V (b) 1.0 V (c) 1 mV (d) 10 mV

Ans. (d)

Current amplification factor

$$\beta = \frac{\Delta I_c}{\Delta I_B}$$

Collector resistance

$$\Delta I_c = \frac{2V}{2 \times 10^3 \Omega} = 1 \times 10^{-3} A$$

Base current

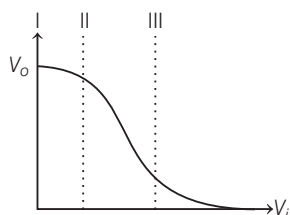
$$\Delta I_B = \frac{V_B}{R_B} = \frac{V_B}{1 \times 10^3} = V_B \times 10^{-3}$$

Given, $\beta = 100$

Now, $100 = \frac{10^{-3}}{V_B \times 10^{-3}}$

$$V_B = \frac{1}{100} V = 10 \text{ mV}$$

- 78** Transfer characteristic [output voltage (V_o) vs input voltage (V_i)] for a base biased transistor in CE configuration is as shown in the figure. For using transistor as a switch, it is used **[CBSE AIPMT 2012]**



- (a) in region III
 (b) both in region (I) and (III)
 (c) in region II
 (d) in region I

Ans. (b)

For using transistor as a switch, it is used in cut-off state and saturation state only.

- 79** A common emitter amplifier has a voltage gain of 50, an input impedance of 100 Ω and an output impedance of 200 Ω . The power gain the amplifier is **[CBSE AIPMT 2010, 2007]**
 (a) 500 (b) 1000
 (c) 1250 (d) 50

Ans. (c)

Concept AC power gain
 $= \frac{\text{change in output power}}{\text{change in input power}}$
 $= \frac{\Delta V_c \times \Delta i_c}{\Delta V_i \times \Delta i_b}$
 $= \left(\frac{\Delta V_c}{\Delta V_i}\right) \times \left(\frac{\Delta i_c}{\Delta i_b}\right) = A_v \times \beta_{AC}$

where, A_v is voltage gain and $(\beta)_{AC}$ is AC current gain. Also,

$$A_v = \beta_{AC} \times \text{resistance gain} \left(= \frac{R_o}{R_i} \right)$$

Voltage gain = $\beta \times$ impedance gain

$$\Rightarrow 50 = \beta \times \frac{200}{100} \Rightarrow \beta = 25$$

Also, power gain = $\beta^2 \times$ impedance gain
 $= 25^2 \times \frac{200}{100} = 1250$

- 80** A transistor is operated in common-emitter configuration at $V_c = 2$ volt such that a change in the base current from 100 μA to 200 μA produces a change in the collector current from 5 mA to 10 mA. The current gain is **[CBSE AIPMT 2009]**
 (a) 75 (b) 100
 (c) 150 (d) 50

Ans. (d)

For a transistor

$$I_E = I_B + I_C$$

where I_E = emitter current

I_B = base current

I_C = collector current

and current gain $\beta = \frac{\Delta I_c}{\Delta I_B}$

Here, $\Delta I_c = 10 \times 10^{-3} - 5 \times 10^{-3}$
 $= 5 \times 10^{-3} A$
 $\Delta I_B = 200 \times 10^{-6} - 100 \times 10^{-6}$
 $= 100 \times 10^{-6} A$
 $\therefore \beta = \frac{5}{100} \times 1000 = 50$

- 81** The voltage gain of an amplifier with 9% negative feedback is 10. The voltage gain without feedback will be **[CBSE AIPMT 2008]**
 (a) 90 (b) 10 (c) 1.25 (d) 100

Ans. (d)

Voltage gain = $\frac{A_v}{1 + \beta A_v}$
 $10 = \frac{A_v}{1 + \frac{9}{100} A_v}$
 $A_v = \frac{10}{0.1} = 100$

- 82** A transistor is operated in common emitter configuration at constant collector voltage $V_c = 1.5$ V such that a change in the base current from 100 μA to 150 μA produces a change in the collector current from 5 mA to 10 mA. The current gain (β) is **[CBSE AIPMT 2006]**
 (a) 67 (b) 75 (c) 100 (d) 50

Ans. (c)

AC current gain β is defined as the ratio of the collector to the base current at constant collector voltage,

$$\beta = \left(\frac{\Delta i_c}{\Delta i_b} \right)_{V_c}$$

Given, $\Delta i_c = 10 \text{ mA} - 5 \text{ mA} = 5 \text{ mA}$

$$\Delta i_b = 150 \mu A - 100 \mu A = 50 \mu A$$

$$\therefore \beta = \frac{5 \text{ mA}}{50 \times 10^{-3} \text{ mA}} = 100$$

In common emitter amplifier, the output voltage signal is 180° out of phase with the input voltage signal

- 83** A transistor-oscillator using a resonant circuit with an inductor L (of negligible resistance) and a capacitor C in series produce oscillations of frequency f . If L is doubled and C is changed to 4 C , the frequency will be **[CBSE AIPMT 2006]**
 (a) $\frac{f}{4}$ (b) $8f$ (c) $\frac{f}{2\sqrt{2}}$ (d) $\frac{f}{2}$

Ans. (c)

In a series LC-circuit, frequency of LC-oscillations is given by

$$f = \frac{1}{2\pi\sqrt{LC}} \text{ or } f \propto \frac{1}{\sqrt{LC}}$$

Considering two cases of L and C,

$$\frac{f_1}{f_2} = \sqrt{\frac{L_2 C_2}{L_1 C_1}}$$

Given, $L_1 = L, C_1 = C, L_2 = 2L, C_2 = 4C, f_1 = f$

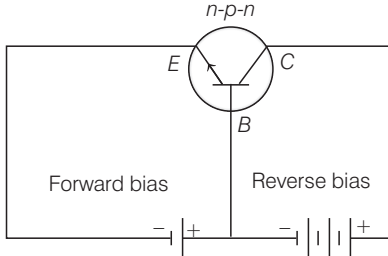
$$\therefore \frac{f}{f_2} = \sqrt{\frac{2L \times 4C}{LC}} = \sqrt{8} \Rightarrow f_2 = \frac{f}{2\sqrt{2}}$$

84 A n-p-n transistor conducts when
[CBSE AIPMT 2003]

- (a) collector is positive and emitter is at same potential as the base
- (b) both collector and emitter are negative with respect to the base
- (c) both collector and emitter are positive with respect to the base
- (d) collector is positive and emitter is negative with respect to the base

Ans. (d)

For amplifying action of a transistor, emitter-base junction is always forward biased while base-collector junction is reverse biased. For forward biasing of emitter-base junction in n-p-n transistor, left n-side i.e. emitter should be connected to negative terminal and p-side (base) should be connected to positive terminal of the battery. On the other hand, in right side, n-side (collector) should be connected to positive terminal of the battery to make base-collector junction reverse biased. The whole situation is shown in the figure for n-p-n transistor



E → Emitter
B → Base
C → Collector

85 For a transistor $\frac{i_c}{i_e} = 0.96$, the current gain in common-emitter configuration is [CBSE AIPMT 2002]
(a) 6 (b) 12 (c) 24 (d) 48

Ans. (c)

Given that the current gain in common base emitter is

$$\frac{i_c}{i_e} = \text{Current gain } (\alpha) = 0.96$$

So, current gain in common emitter configuration is

$$\beta = \frac{\alpha}{1-\alpha} = \frac{0.96}{1-0.96} = \frac{0.96}{0.04} = 24$$

The current gain β in common emitter mode is very large as compared to the current gain α in common base mode. This is why a transistor is always used as an amplifier in the CE mode.

86 In a common-base configuration of a transistor $\frac{\Delta i_c}{\Delta i_e} = 0.98$, then

current gain in common emitter configuration of transistor will be
[CBSE AIPMT 2001]

- (a) 49 (b) 98
- (c) 4.9 (d) 24.5

Ans. (a)

The current gain (α) in common-base configuration is

$$\alpha = \frac{\Delta i_c}{\Delta i_e} \left[\begin{array}{l} \text{at constant voltage across} \\ \text{collector base junction} \end{array} \right] = 0.98$$

The current gain in common-emitter configuration

$$\beta = \frac{\alpha}{1-\alpha} = \frac{0.98}{1-0.98} = \frac{0.98}{0.02} = 49$$

87 If α and β are current gains in common-base and common-emitter configurations of a transistor, then β is equal to [CBSE AIPMT 2000]

- (a) $\frac{1}{\alpha}$ (b) $\frac{\alpha}{1+\alpha}$
- (c) $\frac{\alpha}{1-\alpha}$ (d) $\alpha - \frac{1}{\alpha}$

Ans. (c)

Current gain in common-base configuration is,

$$\alpha = \left(\frac{\Delta i_c}{\Delta i_e} \right)_{V_{cb}} \left[\begin{array}{l} \text{at constant voltage across} \\ \text{collector base junction} \end{array} \right]$$

Current gain in common-emitter configuration is,

$$\beta = \left(\frac{\Delta i_c}{\Delta i_b} \right)_{V_{ce}} \left[\begin{array}{l} \text{at constant voltage across} \\ \text{collector emitter junction} \end{array} \right]$$

Also $i_b = i_e - i_c$
or $\Delta i_b = \Delta i_e - \Delta i_c$
As $\beta = \frac{\Delta i_c}{\Delta i_b} = \frac{\Delta i_c}{\Delta i_e - \Delta i_c} \times \frac{\Delta i_e}{\Delta i_e}$
or $\beta = \alpha \times \frac{\Delta i_e}{\Delta i_e - \Delta i_c}$
or $\beta = \alpha \times \frac{1}{1 - \frac{\Delta i_c}{\Delta i_e}}$ or $\beta = \frac{\alpha}{1-\alpha}$

Alternative As we know that relation between current gain in common base and common emitter configuration is given by

$$\alpha = \frac{\beta}{1+\beta}$$

$$\Rightarrow \alpha + \alpha\beta = \beta \Rightarrow \beta - \alpha\beta = \alpha$$

$$\Rightarrow \beta(1-\alpha) = \alpha$$

$$\Rightarrow \beta = \frac{\alpha}{1-\alpha}$$

β is always greater than α . Also $\alpha < 1$ and $\beta > 1$.

88 The transfer ratio β of a transistor is 50. The input resistance of the transistor when used in the common emitter configuration is 1 k Ω . The peak value of the collector AC current for an AC input voltage of 0.01 V peak is [CBSE AIPMT 1998]

- (a) 100 μ A (b) 0.01 mA
- (c) 0.25 mA (d) 500 μ A

Ans. (d)

Input current or base current is given by

$$i_b = \frac{\Delta V_b}{R_b} = \frac{0.01}{1000} = 10^{-5} \text{ A}$$

$$\left[\begin{array}{l} \Delta V_b = \text{input voltage} \\ R_b = \text{base resistance} \end{array} \right]$$

Also current gain

$$\beta = \frac{i_c}{i_b}$$

$$\therefore i_c = \beta i_b = 50 \times 10^{-5} \text{ A} = 500 \times 10^{-6} \text{ A} = 500 \mu\text{A}$$

89 The correct relationship between the two current gains α and β in a transistor is [CBSE AIPMT 1997]

- (a) $\beta = \frac{1+\alpha}{\alpha}$ (b) $\alpha = \frac{\beta}{1+\beta}$
- (c) $\alpha = \frac{\beta}{1-\beta}$ (d) $\beta = \frac{\alpha}{1+\alpha}$

Ans. (b)

Current gain in common base configuration

$$\alpha = \frac{\Delta i_c}{\Delta i_e}$$

Current gain in common emitter configuration

$$\beta = \frac{\Delta i_c}{\Delta i_b}$$

And as we know that emitter current is equal to sum of base current and collector current

$$\text{So, } i_e = i_b + i_c \Rightarrow \Delta i_e = \Delta i_b + \Delta i_c$$

$$\begin{aligned} \therefore \alpha &= \frac{\Delta i_c}{\Delta i_b + \Delta i_c} \\ &= \frac{\Delta i_c / \Delta i_b}{1 + \frac{\Delta i_c}{\Delta i_b}} = \frac{\beta}{1 + \beta} \end{aligned}$$

or
$$\alpha = \frac{\beta}{\beta + 1}$$

90 The current gain for a transistor working as common base amplifier is 0.96. If the emitter current is 7.2 mA, then the base current is [CBSE AIPMT 1996]

- (a) 0.29 mA (b) 0.35 mA
(c) 0.39 mA (d) 0.43 mA

Ans. (a)

DC current gain in common base amplifier is given by

$$\alpha = \frac{i_c}{i_e}$$

where, i_c is collector current and i_e is emitter current.

$$\text{Given, } \alpha = 0.96, i_e = 7.2 \text{ mA}$$

$$\therefore i_c = 0.96 \times 7.2 \text{ mA} = 6.91 \text{ mA}$$

$$\text{As, } i_e = i_b + i_c$$

$$\therefore \text{Base current } i_b = i_e - i_c = 7.2 - 6.91 = 0.29 \text{ mA}$$

91 When a $n-p-n$ transistor is used as an amplifier, then [CBSE AIPMT 1996]

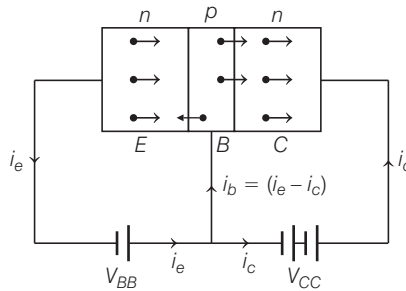
- (a) the electrons flow from emitter to collector
(b) the holes flow from emitter to collector
(c) the electrons flow from collector to emitter
(d) the electrons flow from battery to emitter

Ans. (a)

In $n-p-n$ transistor, electrons are majority carriers in emitter (n -type

semiconductor) and are repelled towards base by negative potential of V_{BB} as emitter base junction is forward biased i_e . The base being thin and lightly doped (p -type semiconductor) has low number density of holes.

When electrons enter the base region, then only a few holes (say 5%) get neutralised by the electron-hole combination, resulting base current ($i_b = 5\% i_e = 0.05 i_e$). The remaining 95% electrons pass over to the collector, on account of high positive potential of collector due to battery V_{CC} , resulting collector current ($i_c = 95\% i_e = 0.95 i_e$)



92 An oscillator is nothing but an amplifier with [CBSE AIPMT 1994]

- (a) positive feedback
(b) negative feedback
(c) large gain
(d) no feedback

Ans. (a)

A transistor amplifier with proper positive feedback can act as an oscillator, i.e. it can generate oscillations without any external signal source. A positive feedback amplifier is one that produces a feedback voltage (V_f) that is in phase with the original input signal. A phase shift of 180° is produced by the amplifier and a further phase shift of 180° is introduced by feedback network. Consequently, the signal is shifted by 360° and fed to the input, i.e. feedback voltage is in phase with the input signal.

93 The part of the transistor which is heavily doped to produce large number of majority carriers is [CBSE AIPMT 1993]

- (a) emitter
(b) base
(c) collector
(d) Any of the above depending upon the nature of transistor

Ans. (a)

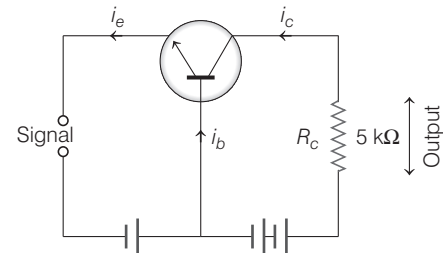
In transistor the emitter is heavily doped, so that it can inject a large number of charge carriers (electrons or holes) into the base. The base is lightly doped and very thin; it passes most of the emitter injected charge carriers to the collector. The collector is moderately doped.

94 To use a transistor as an amplifier [CBSE AIPMT 1991]

- (a) the emitter base junction is forward biased and the base collector junction is reverse biased
(b) no bias voltage is required
(c) both junctions are forward biased
(d) both junctions are reverse biased

Ans. (a)

A transistor raises the strength of a weak signal and thus acts as an amplifier. In order to achieve faithful amplification, the input circuit should always remain forward biased. To do so, a DC voltage is applied in the input circuit in addition to the signal. This DC voltage is known as bias voltage and its magnitude is such that it always keeps the input circuit forward biased regardless of the polarity of the signal.

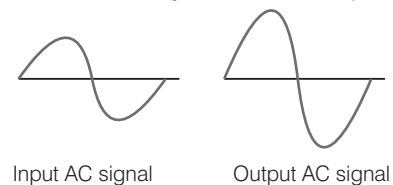


The collector-base junction is reverse biased and has a very high resistance of the order of mega ohms.

95 In a common base amplifier the phase difference between the input signal voltage and the output voltage is [CBSE AIPMT 1990]
(a) zero (b) $\frac{\pi}{4}$ (c) $\frac{\pi}{2}$ (d) π

Ans. (a)

In common base amplifier circuit, the input signal voltage and the output collector voltage are in the same phase.



96 Radiowaves of constant amplitude can be generated with

[CBSE AIPMT 1989]

- (a) FET (b) filter
(c) rectifier (d) oscillator

Ans. (d)

Many electronic devices require a source of energy at a specific frequency which may range from a few Hz to several MHz. This is achieved by an electronic device called an oscillator. An oscillator can produce waves from small (20 Hz) to extremely high frequencies (> 100 MHz).

TOPIC 3 Digital Circuits

97 Which of the following gate is called universal gate?

[NEET (Oct.) 2020]

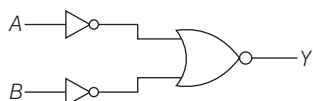
- (a) OR gate
(b) AND gate
(c) NAND gate
(d) NOT gate

Ans. (c)

NAND and NOR gate are called universal gate because all type of logic gates and Boolean expressions can be realised with the help of NAND and NOR gate.

98 For the logic circuit shown, the truth table is

[NEET (Sep.) 2020]



(a)

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

(b)

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

(c)

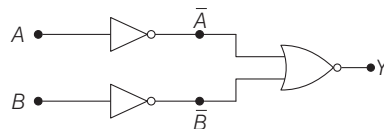
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

(d)

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Ans. (d)

Given, logic circuit is



$$Y = \overline{\overline{A} + \overline{B}}$$

$$= \overline{\overline{A} \cdot \overline{B}}$$

[using de-Morgan's theorem,
 $x + y = \overline{\overline{x} \cdot \overline{y}}$
 $\therefore \overline{\overline{x}} = x$]
 $= A \cdot B$

Truth table for above given logic circuit is

A	B	\overline{A}	\overline{B}	$Y = A \cdot B$
0	0	1	1	0
0	1	1	0	0
1	0	0	1	0
1	1	0	0	1

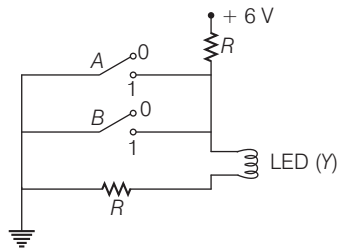
⇒

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Hence, correct option is (d).

99 The circuit diagram shown here corresponds to the logic gate,

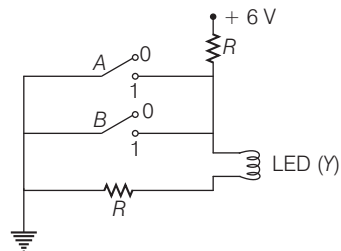
[NEET (Odisha) 2019]



- (a) NOR (b) AND (c) OR (d) NAND

Ans. (a)

From the circuit diagram given below, it can be seen that the current will flow to ground if any of the switch is closed. Also, the LED will only glow when current flows through it.

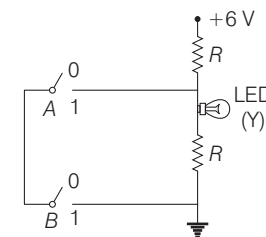


Thus, the truth table for the circuit diagram can be formed as circuit diagram in given solution.

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

The output (Y) is equivalent to that of NOR gate.

100



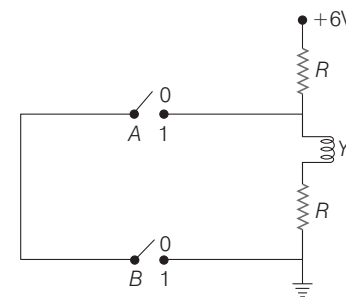
The correct Boolean operation represented by the circuit diagram drawn is

[NEET (National) 2019]

- (a) OR (b) NAND (c) NOR (d) AND

Ans. (b)

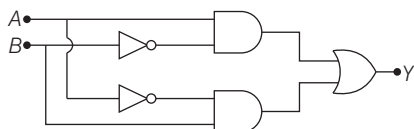
The LED will glow when the current flows through it, i.e. when the voltage across it is high. The truth table can be formed from this



A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

The output Y is same as that come from NAND gate.

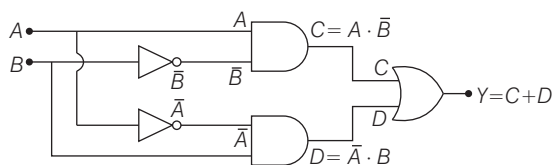
101 In the combination of the following gates the output Y can be written in terms of inputs A and B as [NEET 2018]



- (a) $\overline{A \cdot B} + A \cdot B$ (b) $A \cdot \overline{B} + \overline{A} \cdot B$
 (c) $\overline{A \cdot B}$ (d) $\overline{A + B}$

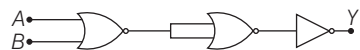
Ans. (b)

According to the question, the figure of combination of gates in terms of inputs and outputs can be given as



Thus, $Y = A \cdot \overline{B} + \overline{A} \cdot B$

102 The given electrical network is equivalent to [NEET 2017]



- (a) AND gate (b) OR gate
 (c) NOR gate (d) NOT gate

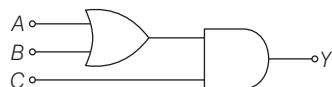
Ans. (c)

Truth table for given network is

A	B	Y_1	Y_2	Y
0	0	1	0	1
1	0	0	1	0
0	1	0	1	0
1	1	0	1	0

Output Y of network matches with that of NOR gate.

103 To get output 1 for the following circuit, the correct choice for the input is [NEET 2016]



- (a) $A=1, B=0, C=0$ (b) $A=1, B=1, C=0$
 (c) $A=1, B=0, C=1$ (d) $A=0, B=1, C=0$

Ans. (c)

Consider the given figure,

The resultant boolean expression of the above logic circuit will be

$$Y = (A + B) \cdot C$$

Now, let us try with inputs A, B and C given in the options and let's see, which one of them will give output 1 at Y .

$$\text{If } A=0, B=0, C=0$$

$$\Rightarrow Y = (0+0) \cdot 0 \Rightarrow Y=0$$

$$\text{If } A=1, B=1, C=0$$

$$\Rightarrow Y = (1+1) \cdot 0$$

$$\Rightarrow Y = 1 \cdot 0 \Rightarrow Y=0$$

$$\text{If } A=1, B=0, C=1$$

$$\Rightarrow Y = (1+0) \cdot 1 \Rightarrow Y = 1 \cdot 1 \Rightarrow Y = 1$$

$$\text{If } A=0, B=1, C=0$$

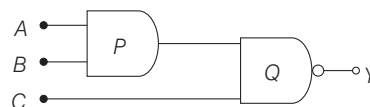
$$\Rightarrow Y = (0+1) \cdot 0$$

$$\Rightarrow Y = 1 \cdot 0 \Rightarrow Y=0$$

So, we have seen that among the given options, only option (c) is the correct choice, i.e.

Output $Y = 1$ only when inputs $A = 1, B = 0$ and $C = 1$.

104 What is the output Y in the following circuit, when all the three inputs A, B, C are first 0 and then 1? [NEET 2016]



- (a) 0, 1 (b) 0, 0
 (c) 1, 0 (d) 1, 1

Ans. (c)

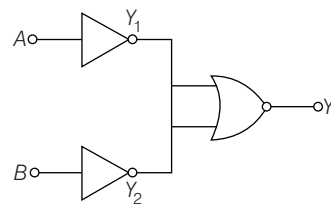
Output of the given circuit is given by

$$y = \overline{(AB)} \cdot C$$

$$\text{When } A=B=C=0, Y_1 = \overline{(0)(0)} \cdot 0 = \overline{0} \cdot 0 = 1 \cdot 0 = 0$$

$$\text{When } A=B=C=1, Y_2 = \overline{(1)(1)} \cdot 1 = \overline{1} \cdot 1 = 0 \cdot 1 = 0$$

105 Which logic gate is represented by the following combination of logic gates? [CBSE AIPMT 2015]



- (a) OR (b) NAND (c) AND (d) NOR

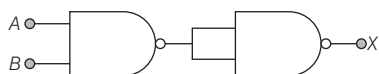
Ans. (c)

The truth table for the given circuit is

A	B	y_1	y_2	$y = \overline{y_1 + y_2}$
0	0	1	1	0
0	1	1	0	0
1	0	0	1	0
1	1	0	0	1

The truth table shows that both the inputs are high, then we are getting high value of output otherwise zero. Hence, the combination represents AND gate.

106 The output (X) of the logic circuit shown in figure will be [NEET 2013]



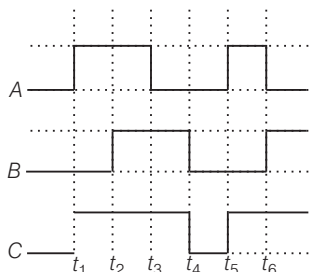
- (a) $X = \overline{A \cdot B}$ (b) $X = \overline{A \cdot \overline{B}}$
 (c) $X = A \cdot B$ (d) $X = \overline{A + B}$

Ans. (c)

(c) $X = \overline{\overline{A \cdot B}} = A \cdot B$ (i.e. AND gate)

If the output of NAND gate is connected to the input of NOT gate (made from NAND gate by joining two inputs) from the given figure then we get back an AND gate.

107 The figure shows a logic circuit with two inputs A and B and the output C. The voltage wave forms across A, B and C are as given. The logic circuit gate is [CBSE AIPMT 2012]



- (a) OR gate (b) NOR gate
 (c) AND gate (d) NAND gate

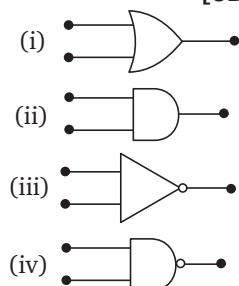
Ans. (a)

From the given waveforms, the following truth table can be made

Inputs		Output
A	B	C
0	0	0
1	0	1
1	1	1
0	1	1

This truth table obtained is of 'OR' gate. So, logic circuit gate is OR gate.

108 Symbolic representation of four logic gates are shown as [CBSE AIPMT 2011]



Pick out which ones are for AND, NAND and NOT gates, respectively.

- (a) (iii), (ii) and (i) (b) (iii), (ii) and (iv)
 (c) (ii), (iv) and (iii) (d) (ii), (iii) and (iv)

Ans. (c)

The symbols given in problem are (i) OR (ii) AND (iii) NOT (iv) NAND

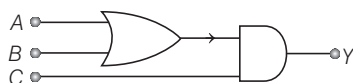
109 The device that can act as a complete electronic circuit is [CBSE AIPMT 2010]

- (a) Junction diode
 (b) Integrated circuit
 (c) Junction transistor
 (d) Zener diode

Ans. (b)

Integrated circuits are miniature electronic circuit produced within a single crystal of a semiconductor such as silicon. They contain a million or so transistors and resistors or capacitors. They are widely used in memory circuits, micro computers, pocket calculators and electronic watches on account of their low cost and bulk, reliability into specific regions of the semiconductor crystals.

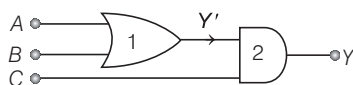
110 To get an output $Y = 1$ from the circuit shown below, the input must be [CBSE AIPMT 2010]



- | | | | | | |
|-------|---|---|-------|---|---|
| A | B | C | A | B | C |
| (a) 0 | 1 | 0 | (b) 0 | 0 | 1 |
| (c) 1 | 0 | 1 | (d) 1 | 0 | 0 |

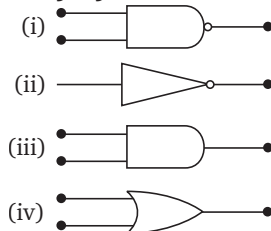
Ans. (c)

Gate I is OR gate, $Y' = A + B$



Gate II is AND gate, $Y = Y' \cdot C$
 $\therefore A = 1, B = 0, C = 1$ will give $Y = 1$

111 The symbolic representation of four logic gates



The logic symbols for OR, NOT and NAND gates are respectively

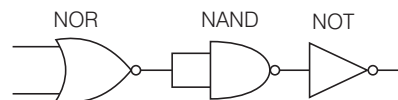
[CBSE AIPMT 2009]

- (a) (iii), (iv), (ii) (b) (iv), (i), (iii)
 (c) (iv), (ii), (i) (d) (i), (iii), (iv)

Ans. (c)

The symbols given in problem are (i) NAND (ii) NOT (iii) AND (iv) OR

112 The circuit is equivalent to [CBSE AIPMT 2008]



- (a) AND gate (b) NAND gate
 (c) NOR gate (d) OR gate

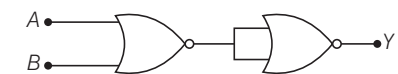
Ans. (c)

The gate circuit can be solved by giving two inputs A and B.

$$\begin{aligned} \text{Output of NOR gate, } Y_1 &= \overline{A + B} \\ \text{Output of NAND gate, } Y_2 &= \overline{Y_1 \cdot Y_1} \\ &= \overline{\overline{A + B} \cdot \overline{A + B}} \\ &= \overline{\overline{A + B} + \overline{A + B}} \\ &= A + B + A + B \\ &= A + B \end{aligned}$$

Output of NOT gate,
 $Y = \overline{Y_2} = \overline{A + B}$
 which is the output of NOR gate.

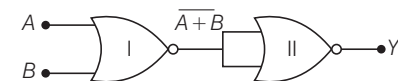
113 In the following circuit, the output Y for all possible inputs A and B is expressed by the truth table [CBSE AIPMT 2007]



- | | | | | | |
|-------|---|---|-------|---|---|
| (a) A | B | Y | (b) A | B | Y |
| 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 0 |
- | | | | | | |
|-------|---|---|-------|---|---|
| (c) A | B | Y | (d) A | B | Y |
| 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 |

Ans. (d)

We can simplify the gate circuit as



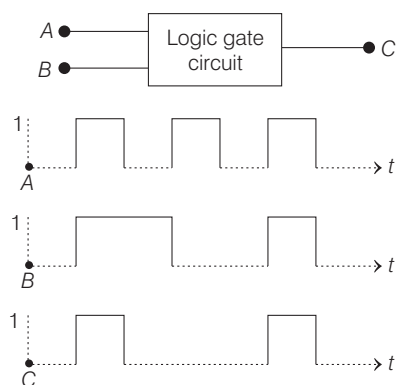
Here, gates-I and II are NOR gates. The output ($\overline{A + B}$) of gate-I will appear as input of gate-II. The final output is

$$Y = \overline{\overline{A + B}} = A + B$$

This is the Boolean expression of OR gate whose truth table is given below

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

114 The following figure shows a logic gate circuit with two inputs A and B and the output C. The voltage waveforms of A, B and C are as shown below



The logic circuit gate is

[CBSE AIPMT 2006]

- (a) AND gate (b) NAND gate
(c) NOR gate (d) OR gate

Ans. (a)

The Boolean expression which satisfies the output of this logic gate is $C = A \cdot B$, which is for AND gate.

115 The output of OR gate is 1

[CBSE AIPMT 2004]

- (a) only if both inputs are zero
(b) if either or both inputs are 1
(c) only if both inputs are 1
(d) if either input is zero

Ans. (b)

OR gate has two inputs A and B and output Y. It follows a logic operation represented by '+'. Thus, its Boolean expression is

$$A + B = Y$$

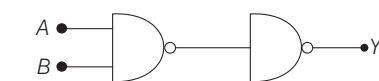
The truth table of OR gate is

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Thus, after observing its Boolean expression and its truth table, it is obvious that output of OR gate is 1 if either or both inputs are 1.

116 Following diagram performs the logic function of

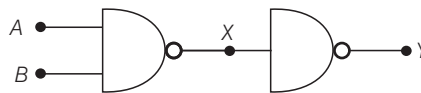
[CBSE AIPMT 2003]



- (a) OR gate (b) AND gate
(c) XOR gate (d) NAND gate

Ans. (b)

For our convenience, the output of first NAND gate is chosen as X as shown



Output of first NAND gate, $X = \overline{A \cdot B}$

Using De-Morgan's theorem

$$\overline{A \cdot B} = \overline{A} + \overline{B}$$

So, $X = \overline{A} + \overline{B}$

Now, output of 2nd NAND gate,

$$Y = \overline{X \cdot X} = \overline{X}$$

Again $\overline{\overline{A} + \overline{B}} = \overline{\overline{A}} \cdot \overline{\overline{B}} = A \cdot B$ ($\because \overline{\overline{A}} = A$)

Hence, $Y = A \cdot B$

This is the logic function of AND gate.

117 The truth table given below

Input		Output
A	B	Y
0	0	0
1	0	0
0	1	0
1	1	1

represents

[CBSE AIPMT 2000]

- (a) AND gate (b) NOR gate
(c) OR gate (d) NAND gate

Ans. (a)

We can see from the truth table that output is 1 only when its both inputs are 1.

This is possible only for AND gate. The Boolean expression for AND gate is

$$Y = A \cdot B$$

which satisfies the truth table as below

$$0 \cdot 0 = 0$$

$$1 \cdot 0 = 0$$

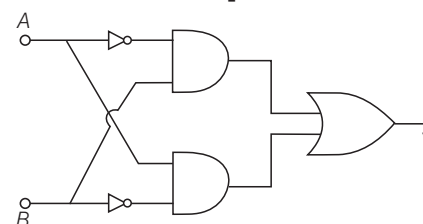
$$0 \cdot 1 = 0$$

$$1 \cdot 1 = 1$$

Here symbol (·) represents AND operation.

118 The following circuit represents

[CBSE AIPMT 1999]



- (a) OR gate
(b) XOR gate
(c) AND gate
(d) NAND gate

Ans. (b)

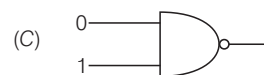
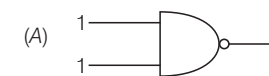
Output of upper AND gate = $\overline{A}B$

Output of lower AND gate = $A\overline{B}$

Thus, output of OR gate = $\overline{A}B + A\overline{B}$

This is Boolean expression for XOR gate.

119 Which one of the following gates will have an output of 1? [CBSE AIPMT 1998]



- (a) A
(c) C

- (b) B
(d) D

Ans. (c)

(a) Gate A is NAND gate, its output will be

$$Y_A = \overline{1 \cdot 1} = \overline{1} = 0$$

(b) Gate B is NOR gate, its output will be

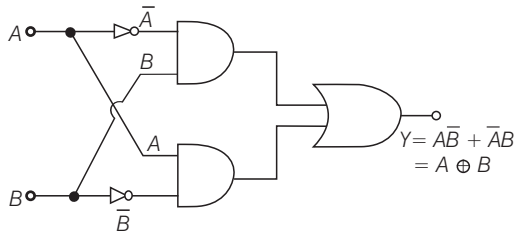
$$Y_B = \overline{1 + 1} = \overline{1} = 0$$

(c) Gate C is NAND gate, its output will be

$$Y_C = \overline{0 \cdot 1} = \overline{0} = 1$$

(d) Gate D is XOR gate, its output will be

$$Y_D = 0 \oplus 0 = 0 \cdot \overline{0} + \overline{0} \cdot 0 = 0$$



Thus, gate(C) will give an output of 1.

120 The following truth table belongs to which of the following four gates? [CBSE AIPMT 1997]

Input		Output
A	B	Y
1	1	0
1	0	0
0	1	0
0	0	1

- (a) NOR (b) XOR
(c) NAND (d) OR

Ans. (a)

The Boolean expression expressed by the truth table may be written as

$$Y = \overline{A + B}$$

This is the expression of NOR gate (OR gate + NOT gate)

NOTE

The NOR gate may be shown as below



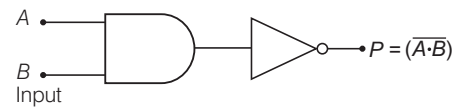
121 Which of the following gates corresponds to the truth table given below? [CBSE AIPMT 1994]

Input		Output
A	B	Y
1	1	0
1	0	1
0	1	1
0	0	1

- (a) NAND (b) OR
(c) AND (d) XOR

Ans. (a)

Truth table for NAND gate is developed by inverting the outputs of the AND gate with NOT gate. Output from a NAND gate is always 1 except when all the inputs are 1. Diagrammatic representation of NAND gate is



122 The following truth table corresponds to the logical gate [CBSE AIPMT 1991]

Input		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

- (a) NAND (b) OR
(c) AND (d) XOR

Ans. (b)

It is clear from the truth table that the output is high if any or all of the inputs are high. The only way to get a low output is by having all inputs low. The output Y of an OR gate is low when all inputs are low. The output Y of an OR gate is high, if any or all the inputs are high. So this truth table is of OR gate.